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EXAMINER

KNOLL, CLIFFORD H

| ART UNIT | PAPER NUMBER |
|----------|--------------|
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2112

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DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/086,665

Applicant(s)

APOSTOL ET AL.

Examiner

Clifford H Knoll

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 July 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-35 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 7/8/2002.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

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DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 16 and 33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 16, "selected" is unclear because the selecting is not positively recited.

In claim 33, the closing semicolon should be a period.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen (US 5197130).

Regarding claims 1 and 10, Chen discloses outbound queues, each of said outbound bus transactions including a bus arbitration priority (e.g., Fig. 14, "326"); and a first state machine coupled to the first and second outbound queues to service the first and second outbound queues, serially requesting for access to the on-chip bus for the staged outbound bus transactions (e.g., Fig. 14, "322"), according the first queue a first outbound priority and the second queue a second outbound priority, where access to the on-chip bus is granted to requesting bus transactions based at least in part on the included bus arbitration priorities of the contending bus transactions (e.g., col. 17, lines 48-51).

Regarding claims 2 and 11, Chen also discloses a configuration register coupled to said first state machine to store said first and second priorities to be accorded to said first and second outbound queues by said first state machine in servicing said first and second outbound queues (e.g., col. 18, lines 4-9).

Regarding claims 3 and 12, Chen also discloses a third outbound queue, which in conjunction with said first and second outbound queues, facilitates selective staging of a third and said first and second plurality of outbound bus transactions for the on-chip subsystem, at the choosing of the on-chip subsystem, with each of the outbound bus transactions including a bus arbitration priority; and said first state machine is also coupled to said third outbound queue, and service said third outbound queue, along with said first and second outbound queues, serially requesting for access to the on-chip bus for the staged outbound bus transactions, according the third queue a third outbound priority complementing said first and second outbound priorities accorded to

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the first and second outbound queues, where access to the on-chip bus is granted to requesting bus transactions based at least in part on the included bus arbitration priorities of the contending bus transactions (e.g., Fig. 19b, "368").

Regarding claims 4 and 13, Chen also discloses inbound queues to facilitate selective staging of a first and a second plurality of inbound bus transactions for the on-chip subsystem, at the choosing of originating subsystems of the inbound bus transactions, each of the inbound bus transaction including a bus arbitration priority and being granted access to the on-chip bus based at least in part on the included bus arbitration priority (e.g., Fig. 14; "324") and a second state machine coupled to the first and second inbound queues to service the first and second inbound queues, serially bringing the staged inbound bus transactions to the attention of the on-chip subsystem, according the first inbound queue a first inbound priority and the second inbound queue a second inbound priority (e.g., col. 20, lines 51-56).

Regarding claims 5 and 14, Chen also discloses the configuration register coupled to said second state machine to store said first and second inbound priorities to be accorded to said first and second inbound queues by said second state machine in servicing said first and second inbound queues (e.g., Fig. 14, "320").

Regarding claims 6 and 15, Chen also discloses a third inbound queue, which in conjunction with said first and second inbound queues, facilitates selective staging of a third and said first and second plurality of inbound bus transactions for the on-chip subsystem, at the choosing of originating subsystems of the inbound bus transactions, with each of the inbound bus transactions including a bus arbitration priority, and

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granted access to the on-chip bus based at least in part on the included bus arbitration priority; and said second state machine is also coupled to said third inbound queue, and service said third inbound queue, along with said first and second inbound queues, serially bringing the staged inbound bus transactions to the attention of the on-chip subsystem, according the third queue a third inbound priority complementing said first and second inbound priorities accorded to the first and second inbound queues (e.g., Fig. 19a).

Regarding claims 7 and 17, Chen discloses a first and a second inbound queue to facilitate selective staging of a first and a second plurality of inbound bus transactions for the on-chip subsystem, at the choosing of originating subsystems of the inbound bus transactions, each of the inbound bus transaction including a bus arbitration priority and being granted access to the on-chip bus based at least in part on the included bus arbitration priority (e.g., Fig. 19a, "352"); and a state machine coupled to the first and second inbound queues to service the first and second inbound queues, serially bringing the staged inbound bus transactions to the attention of the on-chip subsystem, according the first inbound queue a first inbound priority and the second inbound queue a second inbound priority (e.g., Fig. 19a, "44").

Regarding claims 8 and 18, Chen also discloses a configuration register coupled to said state machine to store said first and second inbound priorities to be accorded to said first and second inbound queues by said state machine in servicing said first and second inbound queues (e.g., Fig. 14, "320").

Regarding claims 9 and 19, Chen also discloses the third inbound queue (e.g., Fig. 19a).

Regarding claims 16 and 20, Chen also discloses selecting one of a memory controller, a security engine, a voice processor, a collection of peripheral device controllers, a framer processor, and a network media access controller (e.g., col. 10, lines 56-66).

Regarding claims 21 and 27, Chen discloses determining intra-subsystem priorities for transactions with others subsystems of the integrated circuit to be serviced for requesting access to an on-chip bus of the integrated circuit, to which the subsystems are coupled (e.g., Fig. 3, "46"); generating and staging the transactions in accordance with the determined intra-subsystem priorities, including with each of the staged transactions a bus arbitration priority for use to arbitrate for access to the on-chip bus with other inter-subsystem transactions of other subsystems of the integrated circuit (e.g., Fig. 19b); and serially servicing the staged transactions in accordance with their intra-subsystem priorities, requesting access to the on-chip bus for each staged transaction being serviced using the included bus arbitration priority (e.g., Fig. 19b, "362").

Regarding claims 22 and 28, Chen also discloses generating and staging each of the transactions in a selected one of a plurality of outbound queues in accordance with the determined intra-subsystem priorities (e.g., Fig. 14, "322"), including with each of the staged transactions a bus arbitration priority for use to arbitrate for access to the on-chip

bus with other inter-subsystem transactions of other subsystems of the integrated circuit transactions (e.g., col. 17, lines 48-51).

Regarding claim 23, Chen also discloses staging transactions from other subsystems in a priority based manner as requested by originating subsystems of the transactions, each of said transactions from other subsystems having a bus arbitration priority (e.g., Fig. 14, "322") and serially servicing the staged transactions from other subsystems, notifying core logic of the subsystem, in accordance with the priority based manner the transactions from other subsystems are staged (e.g., col. 20, lines 51-56).

Regarding claim 24, Chen also discloses staging each of the transactions from other subsystems in a selected one of a plurality of prioritized inbound queues as requested by the originating subsystems of the transactions (e.g., Fig 19a, "352").

Regarding claim 25, Chen discloses staging transactions from other subsystems in a priority based manner as requested by originating subsystems of the transactions, each of said transactions from other subsystems having a bus arbitration priority (e.g., Fig. 14, "322"), on which access to a on-chip bus the subsystems are coupled was granted; and serially servicing the staged transactions from other subsystems, notifying core logic of the subsystem, in accordance with the priority based manner the transactions from other subsystems are staged (e.g., col. 20, lines 51-56).

Regarding claim 26, Chen also discloses staging each of the transactions from other subsystems in a selected one of a plurality of prioritized inbound queues as requested by the originating subsystems of the transactions (e.g., Fig 19a, "352").

Regarding claims 29 and 30, Chen also discloses the inbound queues to facilitate selective staging of a first and a second plurality of inbound bus transactions for core logic of the particular subsystem, at the choosing of originating subsystems of the inbound bus transactions, each of the inbound bus transaction including a bus arbitration priority and being granted access to the on-chip bus based at least in part on the included bus arbitration priority (e.g., Fig. 14, "326"); and a second state machine coupled to the first and second inbound queues to service the first and second inbound queues, serially bringing the staged inbound bus transactions to the attention of the core logic of the particular subsystem, according the first inbound queue a first inbound priority and the second inbound queue a second inbound priority (e.g., col. 17, lines 48-51).

Regarding claim 31, Chen also discloses selecting one of a memory controller, a security engine, a voice processor, a collection of peripheral device controllers, a framer processor, and a network media access controller (e.g., col. 10, lines 56-66).

Regarding claim 32, Chen discloses first and second subsystems each having a data transfer interface initiating transactions with other subsystems through selective employment of facilities of the data transfer interface to internally prioritizing the order the transactions are to be serviced by the data transfer interface (e.g., Fig 19b), and including with said first transactions first bus arbitration priorities to facilitate prioritization of granting of access to the on-chip bus to contending inter-subsystem transactions including said first transactions (e.g., col. 17, lines 48-51).

Regarding claim 33, Chen also discloses the first data transfer interface of the first subsystem staging third transactions from other subsystems in a priority based manner as requested by originating subsystems of the third transactions, said third transactions from other subsystems also having third bus arbitration priorities, based on which accesses to said on-chip bus were granted (e.g., Fig 19a, "44").

Regarding claim 34, Chen also discloses the first data transfer interface of the first subsystem serially servicing the staged third transactions from other subsystems, notifying core logic of the first subsystem, in accordance with the priority based manner the third transactions from other subsystems are staged (e.g., Fig 19a, "44").

Regarding claim 35, Chen also discloses the second data transfer interface of the second subsystem staging fourth transactions from other subsystems in a priority based manner as requested by originating subsystems of the fourth transactions, said fourth transactions from other subsystems also having fourth bus arbitration priorities, based on which accesses to said on-chip bus were granted (e.g., Fig 19a, "44").

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Zuravleff (US 5812799) also discloses inbound and outbound queue structures.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H Knoll whose telephone number is 703-305-8656. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



chk

Khanh Dang
Primary Examiner